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Why all the buzz about SOI?

Silicon-on-insulator technology offers solutions to the higher-performance and lower-power dilemma

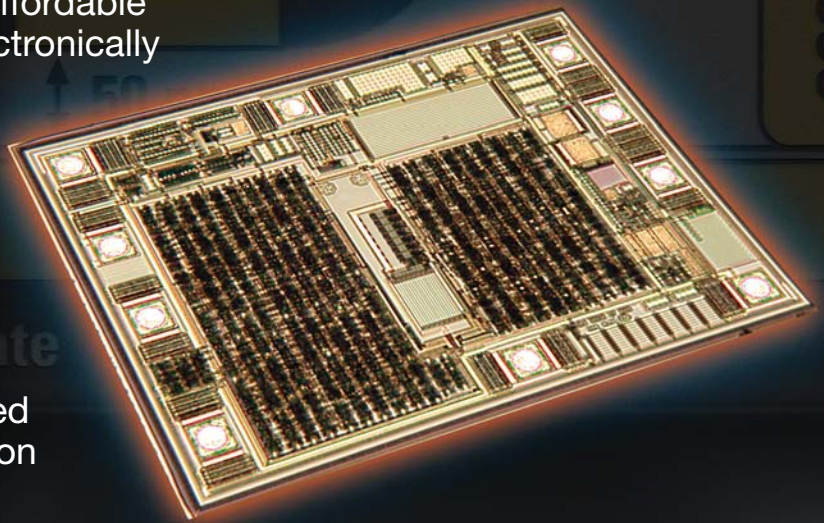
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Why all the buzz about SOI?

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By Don Corson and Pierre Delatte

The advantages of silicon on insulator (SOI) have been known for quite some time and it has been used in specialized applications for many years. It is, however, only recently that semiconductor manufacturers have realized that SOI offers solutions to many of the problems they face in the race to higher performance and lower power. At the same time, SOI does not require major changes to the well-known and well-mastered complementary metal oxide semiconductor (CMOS) process flow.

SOI's use in very high speed microprocessors is well known and many articles have appeared about this application. This article will highlight SOI's less well know features and many of the applications that these features improve or make possible, such as:

- RF identification (RFID) reading distance;
- RF applications;
- Supervisory circuits ultra low voltage;
- High-temperatures and harsh environments;
- Optical and blue light applications;
- Magnetic sensors low noise; and
- Watches and hearing aids with extremely low power.

SOI advantages

SOI is known for offering two major advantages: high speed and low power consumption. These two factors are pushing the development of SOI in many fields and product groups, including the high visibility applications in microprocessors with gigahertz clock rates.

However, these are not the only advantages of SOI. *Fully depleted SOI* (FD-SOI) has improved electrical characteristics compared to bulk CMOS, allowing optimization for high temperature and extremely low voltage/low power applications.

Partially depleted SO (PD-SOI), on the other hand, is optimal for high speed and is being targeted for applications where highest

clock rates are needed as in the above-mentioned applications.

It can be seen in Figure 1 that, compared to a bulk process, SOI offers reduced capacitance and no leakage path to the substrate.

Because the SOI structures are inherently insulated, they can also be packed closer together, offering up to a 15 percent increase in circuit density, reducing the circuit size, and helping to offset the increased cost of SOI substrate material.

PD and FD SOI

The two types of SOI devices, PD-SOI and FD-SOI, refer to the character of the depletion in the gate region. In partially depleted processes, the thickness of the active silicon layer is greater than the depletion width under the gate, leaving a neutral region that extends down to the buried oxide insulation layer.

This neutral region gives PD-SOI devices unique characteristics caused by the so-called floating body effects (FBE). These "parasitic" effects can be used to increase the operating frequency of the devices. On the other hand, substantial efforts are needed when transferring bulk CMOS designs to PD-SOI to allow for these effects.

In FD-SOI devices, the active silicon layer is thin enough that the depletion width extends completely to the underlying oxide layer. Because of this the subthreshold slope of the device is steeper, nearing the theoretical value of 63 mV/dec.

This characteristic allows reducing the leakage current at the same threshold voltage (V_{th}), reducing V_{th} , or a combination of the two. At the same time the $1/f$ noise can be reduced by more than one decade and the temperature characteristic of V_{th} is improved to approximately 0.8 mV/degree K, which provides the basis for the high temperature capability of FD-SOI. FD-SOI does not have the FBE of PD-SOI, which allows transferring designs from bulk processes in a more straightforward manner.

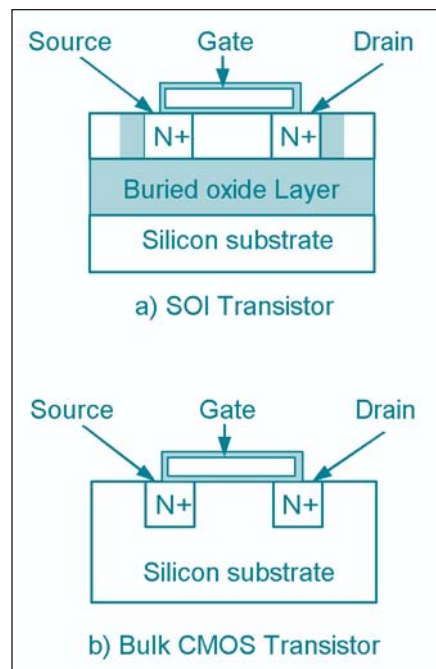


Figure 1: SOI offers reduced capacitance and no leakage path to the substrate.

In production, FD-SOI devices require carefully controlling the silicon thickness, with values in the order of 50 nm. The electrical parameters of the device are dependent on this thickness. Very high uniformity is required. This presents a major challenge. Only more specialized semiconductor production facilities have announced FD-SOI.

PD-SOI devices, on the other hand, can be manufactured on standard bulk CMOS production lines.

FD-SOI applications

As can be seen from above, FD-SOI offers the most particular advantages for performance driven products, including the following areas.

RFID

RFID products, contactless read and writable badges and tags for access control and unit identification, are finding ever-increasing application fields.

These products are divided in two groups, passive and active tags. Active tags include a battery for the necessary energy, such as the tags used widely on the U.S. East Coast for paying road tolls, known as *EZpass*. These tags are, however, large and expensive.

The more interesting group is the passive tag, in which the energy needed for the chip power supply is transferred in the electric or magnetic field that is also transferring the data. For passive tags, the extreme low voltage capabilities of FD-SOI will allow dramatic improvements in product performance,

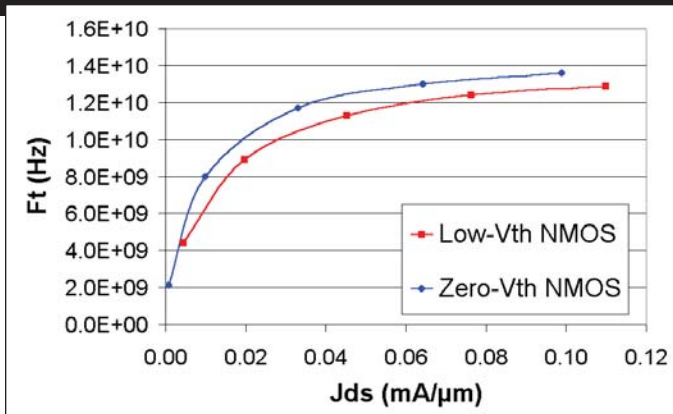


Figure 2: F_t versus the current density for multi-fingers RF transistor in $0.5 \mu\text{m}$ FD-SOI ($V_{ds} = 1.5 \text{ V}$; $n_x W_x L_g = 10 \mu\text{m}^2 \times 12 \mu\text{m}^2 \times 0.5 \mu\text{m}^2$) with low- and zero- V_{th} .

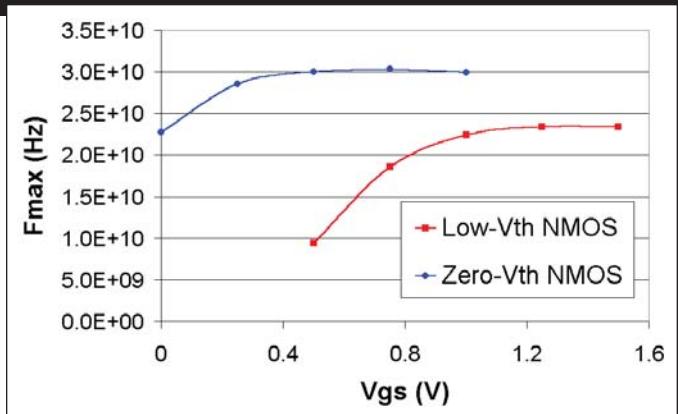


Figure 3: F_{max} versus V_{gs} for multi-fingers RF transistor in $0.5 \mu\text{m}$ FD-SOI ($V_{ds} = 1.5 \text{ V}$; $n_x W_x L_g = 10 \mu\text{m}^2 \times 6 \mu\text{m}^2 \times 0.5 \mu\text{m}^2$) with low- and zero- V_{th} .

especially in the UHF band (400 MHz to 900 MHz), such as supported by EM4222, and in the microwave (2.45 GHz and up) band.

Conventional passive tags and labels in these frequency ranges are limited in their range by the low impedance characteristics of their antennas, which limit the voltage that can be produced. A 30 percent increase in communications range can be expected using the same antennas on FD-SOI parts.

Examples include applications in the laundry industry that allow reading the tags on whole vats of cleaned textiles, or to prevent counterfeiting by allowing positive identification of a garment at the point of sale.

A new application that can be addressed using FD-SOI tags is high temperature tags for logistics applications in paint shops where it is necessary to read the IDs of the tagged parts during the curing of the paint at temperatures of around 220°C .

RF applications

FD-SOI technology offers a number of advantages for RF circuit design with respect to BULK. It is considered the best candidate to achieve ultra-low-voltage and ultra-low power operation¹. Sub-1 V RF circuits have been demonstrated using SOI^{2,3}.

The current gain cut-off frequency F_t of FD-SOI devices is slightly improved thanks to better g_m . The maximum oscillation frequency F_{max} , the most relevant figure of merit for RF transistors, is much better for FD-SOI than for BULK thanks to a reduction of parasitic capacitances.

Figure 2 and Figure 3 show F_t and F_{max} for $0.5 \mu\text{m}$ FD SOI devices. F_{max} up to 30 GHz are achieved at low bias voltage with intrinsic (zero- V_{th}) negative metal oxide semiconductors (NMOS) transistors, which are standard in FD-SOI processes. They use the intrinsic doping of the SOI layer, and are fabricated by masking the channel implant. The F_{max} performances are at least comparable with $0.35 \mu\text{m}$ bulk CMOS. Moreover, intrinsic transistors show an increase of F_t for a given current consumption.

SOI technology also allows improving the quality of passive devices. The reduction of parasitic capacitances increases the tuning range of MOS varactors. LC-tuned voltage controlled oscillators (VCOs) with larger frequency tuning can be designed in SOI, making them more robust to process variations⁴. Clever SOI design allows increasing the quality factor of varactors⁵.

SOI technology is compatible with the use of high-resistivity substrates (greater than 1000 ohm.cm). This improves the substrate isolation (20 dB at 1 GHz) with respect to standard-resistive substrates (10 ohm.cm)⁶ and increases the quality factor of integrated planar inductors thanks to reduced substrate losses. Figure 4 shows the influence of substrate resistivity on the quality factor of a 1.5 nH spiral inductor.

Finally, SOI permits to realize high-performance Tx/Rx switches. The reduction of parasitic capacitances and the use of high-resistive substrates allow reducing the insertion loss while increasing the isolation⁷. Note that the insertion loss of a switch included between the antenna and the low noise amplifier (LNA) is directly added to the noise figure of the receiver chain.

Supervisory circuits

As the voltage levels used in microprocessors and other logic ICs is reduced as a result of the continuing reduction in semiconductor feature size, it will be necessary to have supervisory circuits, resets, and watchdogs guaranteed to work at even lower voltage levels.

By the year 2005, it is expected that the power supply voltage for leading edge semi-

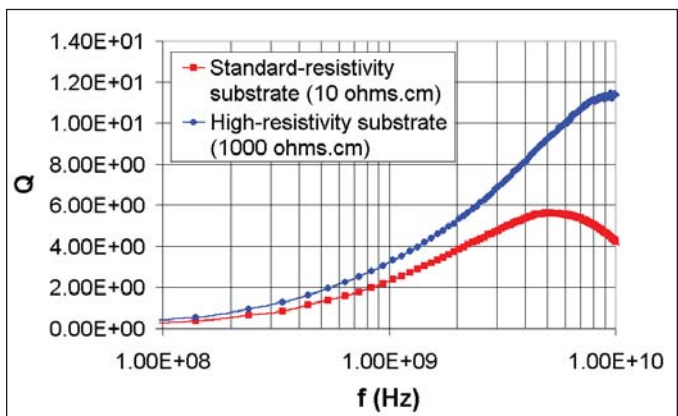


Figure 4: Quality factor of a 1.5 nH spiral inductor on standard- and high-resistivity substrates.

conductor devices will be 1.2 V. For these high volume products, supervisory circuits operating at around 0.6 V will be necessary. Present FD-SOI developments include voltage-reset circuits characterized to run with reset thresholds down to 0.7 V.

High temperature

High temperature is a large value market that has been difficult to serve up until now. In automotive electronics, on-engine and on-transmission applications are projected to require maximum temperatures of up to 200°C with the wheel-mounted applications going even higher. These applications include engine control, transmission control, antilock brake system (ABS), active suspension and wheel speed sensors.

Further high temperature application areas include aerospace and environmental monitoring, such as mining and well logging. The excellent analog properties of FD-SOI devices, along with their low noise, make them predestined for these signal conditioning and mixed mode applications.

A system in which both the sensor and control electronics are fabricated in SOI technology would allow the complete assembly to reside in a thermally harsh environment. This

would allow cost and weight reduction by eliminating requirements for cabling for remotely located electronics.

Optical

Optical sensors form the heart of the present digital imaging boom. Products range from camcorders to still digital cameras, and PC cameras to fax machines and scanners. In this quickly growing market, one of the main limitations of present products is their limited working temperature range, in general from 0° C to +40° C. With SOI, higher temperature sensors are possible along with a reduction in power consumption. A further advantage is a reduction of inter-pixel cross talk, allowing the pixels to be formed closer together.

The so-called *blue light applications* at very low light levels will profit from FD-SOI's inherently low noise levels. These devices can also be made infrared-immune, eliminating blinding from heat sources. The ability to produce the light detector on one side of the oxide barrier and the amplifying circuitry on the other allows increasing the proportion of sensor area on active sensors.

Magnetic sensors

Often needed in metering applications, magnetic sensors will profit from the reduced switching noise of SOI devices. This switching noise has been shown to decrease by a factor of six compared to bulk CMOS. The high temperature qualities of SOI could also be important for this application, possibly opening new markets in automotive and industrial applications.

Extremely low power applications

Watches and hearing aids are among the products that can profit from electronics with extremely low power consumption.

The use of DSPs in hearing aids has been a major breakthrough in increasing hearing quality. The filtering algorithms can easily be trimmed to best match the hearing impairment of each patient. Battery lifetime is, as with most portable equipment, a strong marketing issue that could be addressed using FD-SOI technology. At the same time, the sound quality will be improved by SOI's reduction in 1/f noise by a factor of 10.

Watches offer several different product tracks for lowest power semiconductors.

Increasing the battery lifetime of a watch to five to eight years could make a watch with a hermetic case practical, where the battery is not changeable. This would open a door for very inexpensive diving watches, for example.

Even mechanical watches, without batteries, will profit from ultra low power semiconductors. Using a micro-generator in place of the escapement of a classical mechanical watch opens the door to quartz watch preci-

sion for mechanical watches. The micro-generator will produce the energy needed to power the electronics, which includes a quartz time base, and at the same time function as the escapement, braking the gear train of the watch as necessary.

SOI issues

Compared to BULK process, FD-SOI introduces new technical challenges in production uniformity. Oxide layer thickness and mask-to-mask alignment are especially important. Especially sensitive is the area below the poly gate where differences in thickness or positioning can introduce large fluctuations in parameter values, such as V_{th} and swing. Further, the linear current can be affected and asymmetrical drive behavior can appear. These challenges can all be met with appropriate quality measures.

In production, PD-SOI is non-problematic. However, it does require new engineering models that take the FBE into account. These effects are not only controllable, but also usable to increase the switching speed. PD-SOI is, thus, used in many of today's fastest microprocessor chips.

A further issue with SOI technology is the cost and quality of the wafer material with the buried oxide layer. There are presently two processes used for producing such wafers; separation by implantation of oxygen (SIMOX), and wafer bonding.

Despite great improvements in the quality of SOI wafers these wafers remain more expensive and have more defects than standard wafers. The cost increase is in the range of 10 percent to 20 percent of the fully processed wafer cost, which eliminates SOI for cost-sensitive applications.

Conclusion

SOI technology offers many advantages for tomorrow's performance driven products. Fine-tuning the semiconductors parameters allows chips that work in extreme environments, including extremely low power consumption and very low noise.

This allows further refining of the definition of "application specific integrated circuits" for future products. Custom designs will not only make non-standard products using available technology, but will also be able to choose the parameters necessary to produce a winning product.

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